G.709 OTN Mapping Jitter

Introduction

Asynchronous mapping of Constant Bit Rate (CBR) clients, like SONET or SDH requires the adaptation of the bit rates of SONET/SDH to the asynchronous OTUk bit rate using byte stuffing mechanism. As a consequence of such a justification process phase steps of ± 8 UI are introduced. In principle one additional or one less data byte causes a phase step of 8 UI. In some cases even bursts of n x 8 UI may be generated in consecutive OTUk frames. Since the frame period (e.g about 12 µs for OTU2) is small compared to the time constant of the output clock recovery such a burst can be considered as one single phase step of n x 8 UI. In the demapping process the original clock of the CBR client signal is reconstructed. The data signal is read out under control of a smoothed (equally spaced) clock. Due to the n x 8 UI phase steps in the data stream a certain amount of jitter remains, depending on the frequency of the justification (stuffing) events and on the low-pass characteristics of the clock recovery circuit. In ITU- T Recommendation G.8251 a bandwidth of max. 300 Hz is specified for the CBR output clock. Low frequent justification rates cannot be smoothed out completely, high jitter amplitudes in the low frequency range are still present. All the more, not properly equidistant justification events can generate much higher jitter amplitudes than 8 UI. The jitter measurement high-pass function attenuates those low frequency components accordingly. However they are present at the phase detector of the jitter tester and may cause undesired impairments and incorrect measurement results, e.g. due to overload of the phase comparator. Figure 1 depicts the functional blocks involved in jitter generation and detection of mapping jitter. Figure 2 shows the effect of these functions on the phase signal and the corresponding jitter result.

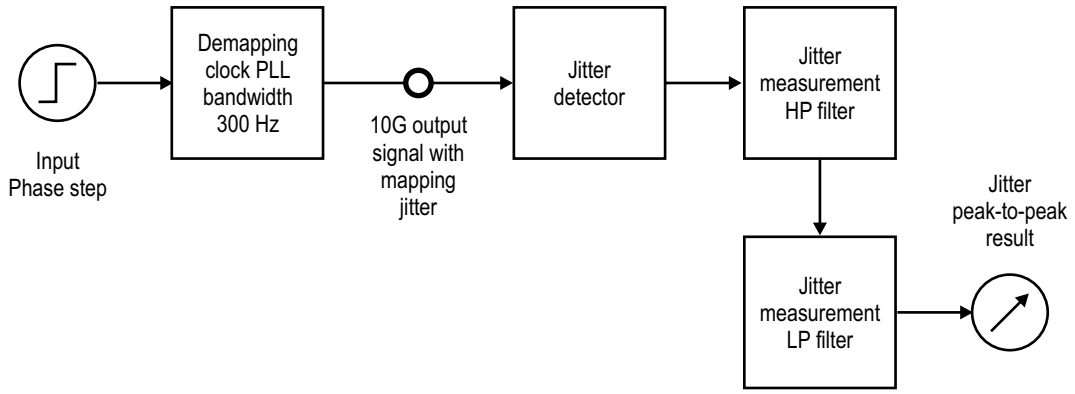

Figure 1: Functional blocks involved in OTN mapping jitter

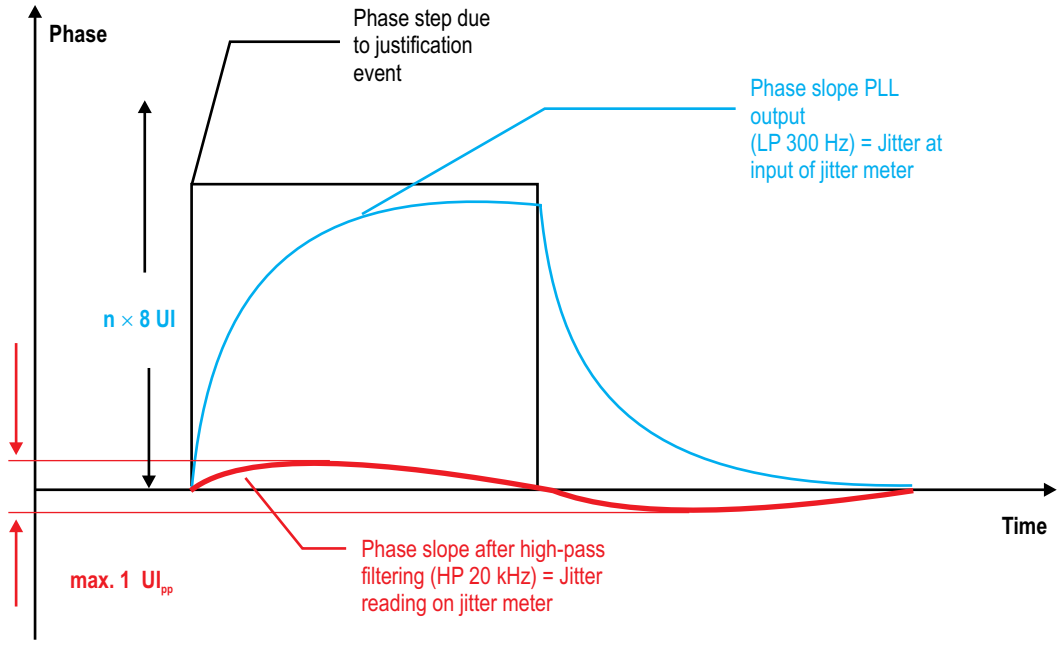

Figure 2: Input/output phase signals and jitter measurement result

Mapping jitter test application

Figure 3 shows a typical test application, where the above mentioned high jitter test signals are present at the 10 Gbit/s SONET/SDH output of the DUT. Particularly at small offset values low frequent justification events are generated. The measurement should therefore be made with different offset values. To configure defined test conditions the ONT-50 Tx should be synchronized to the OTU2 clock if available. The maximum allowed output jitter of the DUT at 10 Gbit/s is specified in ITU-T Recommendation G.8251.

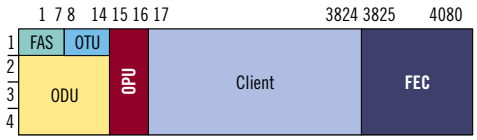

Figure 3: Mapping jitter test configuration

To avoid incorrect jitter measurement results in this critical test application the ONT-50 provides a particular measurement function “Extended 4 UI Range”, which guarantees accurate jitter results, even if high, but low frequent jitter amplitudes complicates the evaluation.

Verification of mapping jitter measurement capability

How to prove a jitter meter if it is capable to measure accurately OTN mapping jitter? In ITU-T Recommendation O.172 phase tolerance tests are defined for jitter meters appropriate for measurement of mapping jitter at PDH tributary outputs. Equivalent sinusoidal signals are specified, which simulate worst case conditions with regard to maximum phase slopes and amplitudes.

The same considerations can be applied to OTN mapping jitter measurements. Starting point is the maximum allowed peak-to-peak jitter of 1.0 UIpp measured with the high-pass filter 20 kHz (STM-64) as specified in Table A.3/G.8251. Taking into account a sine wave with a zero crossing phase slope nearly equivalent to the slope of a phase step filtered by the 300 Hz first order low-pass of the demapper clock recovery (blue curve) leads to a frequency of 300 Hz as shown in Figure 4 (red curve). The 20 kHz first order high-pass jitter filter has an attenuation of 36.5 dB for 300 Hz. For a jitter result of 1.0 UIpp the peak-to-peak amplitude of a 300 Hz sinusoidal signal would be 67 UIpp. Concerning phase steps of multiples of 8 UI it is suggested to apply an equivalent sine wave of 64 UIpp. In this case the ideal jitter result should be 0.96 UIpp ± the accuracy tolerance.

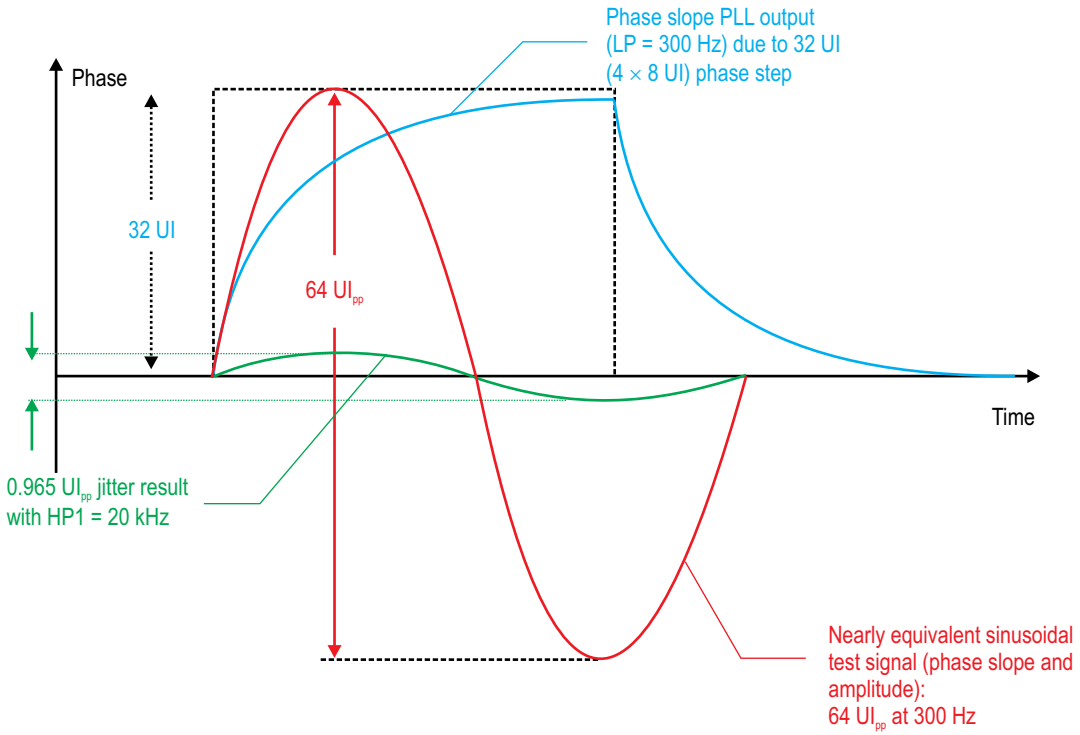

Figure 4: Equivalent sinusoidal phase tolerance.

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