SV2C Personalized SerDes Tester

Product Brief

8 Lane, 28 Gbps USB Modular Instrument for SerDes Validation

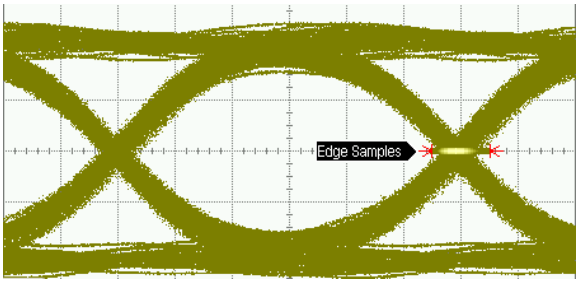
Highly-integrated 28 Gbps parallel tester that meets the emerging test requirements for massive data collection at high speeds. Featuring 8 independent receivers and 8 independent transmitters, the SV2C offers a truly flexible solution for the verification and validation of next generation telecommunications interfaces, and it satisfies a growing need for parallel, system-oriented testing.

Key Features:

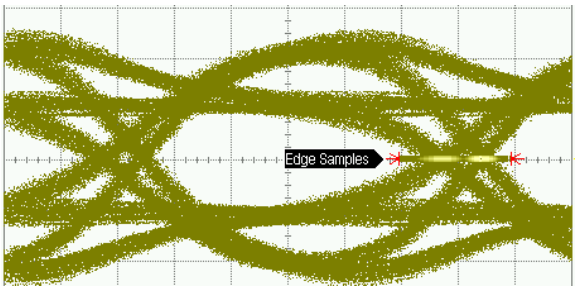
- **Data rates:** 19 Gbps to 28 Gbps fully-continuous operating range.
- **Lanes:** 8 Tx and 8 Rx, differential with per channel adjustment of voltage and timing.
- **DUT Tx/Rx measurements:** eye diagram, EQ, jitter, voltage sensitivity.
- **Ease of use:** the ESP software provides both interaction for debug and automation for fast and comprehensive data collection.
- **Ultra compact size:** for deployment in dense laboratory or production environments.

Key Benefits:

- **Parallel:** a truly parallel system allows for the most comprehensive "stress test" that is possible. The SV2C tests complete 28 Gbps links simultaneously.
- **Self Contained:** an all-in-one system reduces bench space and helps create a portable test and measurement solution; SV2C integrates multiple tools into one.
- **Automation:** Scripting capability is ideal for debug tasks, verification and full-fledged production screening.



28 Gbps Parallel PRBS Eye
(0.4 ps RJ typical using DCA-X PTB/CDR)



28 Gbps Parallel De-Emphasis Eye
(illustrating linear channel)

Pattern Generator Functions

Feature	Description	Benefit
Pattern Generators	Per lane pre-built patterns, PRBS (5, 7, 9, 11, 15, 23, 31), custom user-defined pattern (up to 2 Mb), nested pattern sequencers (up to 16 sequencer programs)	Allows for flexible stimulus generation (e.g. training sequences or compliance patterns)
Analog Controls	Per lane, polarity inversion, voltage swing, 3-tap transmit pre-emphasis, bit-slip up to +/- 20 UI	Provides deep receiver stress characterization with truly independent multi-variable analysis

BERT and Scope Functions

Feature	Description	Benefit
Error Detectors	BERT engines work with all types of patterns listed under Pattern Generator section; single-shot (up to 2^{32} cycles) or continuous error counting modes; 32-bit error counters; automatic pattern alignment	Optimized architecture for production testing and data collection, ensuring rapid pattern alignment and error checking
Equalizer Control	Per lane continuous-time linear equalizers	Allows for design exploration, de-embedding, and correlation with simulation
Clock Recovery	Per-lane analog, hardware clock recovery unit with optimized connection to sampling circuitry	Offers a realistic test environment on any production ATE load board
Analysis Capability	Identify pattern; BERT measurement; BERT scan; eye diagram; analog waveform capture; jitter separation; transition & non-transition eyes	Rapid signal integrity analysis functions behind each transceiver channel

Lanes and Clocking

Feature	Description	Benefit
Lane Count	8 independent generator channels; 8 independent analyzer channels	Allows for truly parallel test
Clock Generators	Two programmable sub-rate clocks	Allows for synchronization with device
Clock References	Internal oscillator (no external clock) or external clock reference with built-in jitter cleaning	Allows for operating the SV2C as a synchronization master or as a synchronization slave

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